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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/698,157	RIBLING, STEVEN K.	
	Examiner	Art Unit	
	Isaac T. Tecklu	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on 09/18/2007.

2. Claims 1, 6 and 11-18 have been amended.

3. Claims 1-23 have been examined.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Richardson (US 7,146,572 B2).

Per claim 1 (Currently Amended), Richardson discloses a data-empowered test program architecture stored on a computer readable storage medium, (e.g. FIG. 3 and related text) comprising:

~~at least one~~ a plurality of control files, each control file defining a test sequence and instructions for executing the test sequence (col. 1:29-62 "... Test module and Sequence File- A file that contains the definition of one or more sequences ..." and e.g. FIG. 3, 212, 220 and "Sequence Files" and related text);

a test executive module configured to ~~determine which~~ select a test sequence to use based on ~~the at least one control file~~ a unit-under-test; (col. 10: 2-50 "... determine whether to execute a step ... " and col. 6: executive sequence may be operable to perform one or more test of the unit- under- test..." and e.g. FIG. 3, element 220 "Test Executive Engine" and 232 and related text);

a test framework software module configured to receive ~~the~~ a selected test sequence from the test executive software module, ~~and~~ determine how to perform the test sequence and perform the selected test sequence; and ~~based on the instructions in the at least once control file and~~ (col. 6: 60-65 "... test executive software may be operable to receive user input to a GUI ..." and e.g. FIG. 3, 212, 220 and 232 and related text);

a plurality of software components in a software components module (col. 1: 15-25 "... test modules to test unit under test (UUTs) ...") coupled for interaction with the test framework software module and structured for outputting at least one test report (e.g. FIG. 6, 309 execution results and related text and col. 1: 15-25 "... the test modules may interact with one or more

hardware instruments to test the UUT(s) ..." and col. 8: 40-50 "... test executive sequence for unit under test ...").

Per claim 2, Richardson discloses the architecture of claim 1 wherein the test framework software module further comprises a hardware abstraction interface (e.g. FIG. 3, element 232 and related text).

Per claim 3, Richardson discloses the architecture of claim 1, further comprising an external reuse library having one or more test descriptions of common signal types (e.g. FIG. 3, element 240 and related text) and being coupled for generating the control files (e.g. FIG. 3, element 240 and Sequence Files and related text).

Per claim 4, Richardson discloses the architecture of claim 1 wherein the software components module further comprises one or more software components for interfacing between the one or more external control files and one or more of the test executive software module and the test framework software module (e.g. FIG. 3 and related text).

Per claim 5, Richardson discloses the architecture of claim 1 wherein the software components module further comprises a pass/fail analyzer and report generator having one or more modes of pass/fail analysis and test reporting (col. 1: 25-30 "... pass/fail results ...").

Per claim 6 (Currently Amended), Richardson discloses a data-empowered test program architecture stored on a computer readable storage comprising:

~~one or more~~ a plurality of external control files having a list of test identification numbers, each test identification number defining a test sequence and instructions for executing the test sequence (col. 1:45-50 "... Sequence File- A file that contains the definition of one or more sequences ..." and e.g. FIG. 3, 212 and 220 and related text and e.g. FIG. 7, step 353 and FIG. 15A and related text);

a test executive module having an execution engine coupled to receive one or more test identification numbers from the list of test identification numbers based on a unit-under test, the test identification number configured to generate, ~~for generating~~ [[,]] (col. 10: 2-50 "... determine whether to execute a step ... " and e.g. FIG. 3, element 220 "Test Executive Engine" and 232 and related text), as a function of the one or more test identification numbers a plurality of test actions to be performed on [[a]] the unit-under-test as defined in the test sequence; (e.g. FIG. 6, 309 execution results and related text and col. 1: 15-25 "... the test modules may interact with one or more hardware instruments to test the UUT(s) ..." and e.g. FIG. 3, element 220 "Test Executive Engine" and related text);

a test framework module for accessing the plurality of test actions and the instructions, the test framework module configured to perform, based on the instructions, the steps of: (col. 6: 60-65 "... test executive software may be operable to receive user input to a GUI ..." and e.g. FIG. 3, 212, 220 and 232 and related text):

i) determining an identification of one of the test hardware resources associated with a current one of the test action (e.g. FIG. 14 and related text),

ii) retrieving the identification of the associated test hardware resource (e.g. FIG. 7, step 351 and related text),

iii) determining a signal type corresponding to the retrieved test hardware resource identification (e.g. FIG. 3, DATA TYPE and related text),

iv) accessing as a function of the signal type one of the external control files having test hardware resource card-type information (col. 23: 45-50), and

v) determining the test hardware resource card-type information as a function of a card-type identifier (e.g. FIG. 15A and related text).

Per claim 7, Richardson discloses the architecture of claim 6 wherein the test hardware resource card-type information includes routing data and parameters for interfacing with an external hardware driver (e.g. FIG. 15A and related text).

Per claim 8, Richardson discloses the architecture of claim 6, further comprising an external reuse library having a plurality of test descriptions corresponding to a plurality of different test signal types (e.g. FIG. 3, DATA TYPE and related text).

Per claim 9, Richardson discloses the architecture of claim 6, further comprising a plurality of software components for interfacing between the external control files and one or more of the test executive module and the test framework module (e.g. FIG. 3, element 232 and related text).

Per claim 10, Richardson discloses the architecture of claim 9 wherein the plurality of software components further comprises one or more modes of pass/fail analysis and test reporting (col. 1: 25-30 "... pass/fail results ...").

Per claim 11 (Currently Amended), Richardson discloses ~~a data empowered test program architecture~~ computing device, comprising:

means for storing a plurality of test actions; (e.g. FIG. 2, 166 and related text

means for determining [[a]] which test actions of the plurality of test actions are to be performed on one of a plurality of ~~unit under test~~ units-under-test; col. 10: 2-50 "... determine whether to execute a step ... " and e.g. FIG. 3, element 220 "Test Executive Engine" and 232 and related text); means for accessing the plurality of the test actions (col. 1: 15-25 "... test modules to test unit under test (UUTs) ...") ~~and~~

means for determining which instructions to use when ~~for~~ performing the plurality of test actions (e.g. FIG. 6, 309 execution results and related text and col. 1: 15-25 "... the test modules may interact with one or more hardware instruments to test the UUT(s) ...");

means for identifying, based on the instructions, [[a]] test hardware resources associated with a current one of the plurality test ~~action~~ actions (e.g. FIG. 14 and related text); and

means for interfacing with an external hardware driver as a function of identifying the test hardware resources associated with the current one of the plurality of test ~~action~~ actions (e.g. FIG. 3, element 232 and related text).

Per claim 12 (Currently Amended), Richardson discloses the ~~architecture~~ computing device of claim 11 wherein the means for interfacing with an external hardware driver further comprises:

means for determining a signal type corresponding to the identified test hardware resource (e.g. FIG. 3, DATA TYPE and related text);

means for accessing as a function of the signal type an external control file having test hardware resource card-type information contained therein (col. 23: 45-50); and

means for determining the test hardware resource card-type information as a function of a card-type identifier (e.g. FIG. 15A and related text).

Per claim 13, Richardson discloses the ~~architecture~~ computing device of claim 11 wherein the means for generating a plurality of test actions further comprises means for generating the plurality of test actions as a function of one or more test identification numbers received from a list of test identification numbers (e.g. FIG. 15B and related text).

Per claim 14, Richardson discloses the ~~architecture~~ computing device of claim 11 wherein the means for generating a plurality of test actions to be performed on a unit-under-test further comprises means for generating a plurality of control files for configuring software code for generating the plurality of test actions (e.g. FIG. 3, element 240 and Sequence Files and related text).

Per claim 15, Richardson discloses the ~~architecture~~ computing device of claim 14 wherein the means for generating a plurality of control files further comprises means for generating one or more of the control files as a function of one or more test descriptions of signal types contained in an external reuse library (e.g. FIG. 3 and related text).

Per claim 16, Richardson discloses the ~~architecture~~ computing device of claim 11, further comprising means for performing pass/fail analysis (col. 1: 25-30 "... pass/fail results ...").

Per claim 17, Richardson discloses the ~~architecture~~ computing device of claim 16, further comprising means for generating one or more test reports.

Per claim 18 (Currently Amended), this is the computer program product version of the claimed architecture discussed above (Claim 11), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Richardson.

Per claim 19 (Currently Amended), this is the computer program product version of the claimed architecture discussed above (Claim 12), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Richardson.

Per claim 20 (Currently Amended), this is the computer program product version of the claimed architecture discussed above (Claim 13), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Richardson.

Per claim 21 (Currently Amended), this is the computer program product version of the claimed architecture discussed above (Claim 16), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Richardson.

Per claim 22 (Currently Amended), this is the computer program product version of the claimed architecture discussed above (Claim 17), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Richardson.

Per claim 23 (Currently Amended), this is the computer program product version of the claimed architecture discussed above (Claim 14), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Richardson.

Response to Arguments

6. Applicant's arguments filed 03/21/2007 have been fully considered but they are not persuasive.

In the Remark, the Applicant argues:

Richardson fails to disclose at least a plurality of control files defining a plurality of test sequences and a test executive configured to select a test sequence from one of the control files (page 10).

Examiner's Response:

The examiner respectfully traverses. Richardson teaches Test Executive Engine 220 which is configured to select different files through the Adapter interface 232. The Test Executive Engine accesses Sequence Adapter to select Sequence Files. The test executive software of FIG. 3 also includes a sequence editor 212 for creating and editing test executive sequences. The sequence editor 212 and the operator interface programs 202 interface to the test executive engine 22 (FIG. 3, Test Executive Engine 220 and Sequence Files and col. 8:25-35).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Isaac T. Tecklu whose telephone number is (571) 272-7957. The examiner can normally be reached on M-TH 9:300A - 8:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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